Claims

1. A method for executing a simulation of a hardware device, the method comprising the steps of:

providing at least one update object having update initialization criteria;

providing at least one hardware object simulating functionality associated with at least one hardware device, the at least one hardware object being responsive to the at least one update object;

providing at least one master object in communication with the at least one update object and the at least one hardware object;

advancing, by the master object, the at least one update object by a predetermined increment; and

executing the at least one hardware object based at least in part on the incremented update object.

2. The method of claim 1 wherein the update object comprises a clock object.

3. The method of claim 1 wherein the update object comprises a level object.

4. The method of claim 1 wherein the update object comprises an arbitrary function object.

5. The method of claim 2 wherein the update initialization criteria comprise at least one of a clock period, a clock duty cycle, a clock initial value, and a clock offset.

6. The method of claim 3 wherein the update initialization criteria comprise at least one of a level initial value and a level transition time.

7. The method of claim 4 wherein the update initialization criteria comprise a

predetermined value corresponding to a predetermined time.

8. The method of claim 1 further comprising at least one transactor object associated with the hardware object.

9. The method of claim 1 wherein the predetermined increment varies based at least in part on the at least one update object.

10. The method of claim 1 wherein the execution step comprises updating an interconnection object in communication with the at least one hardware object.

11. The method of claim 1 wherein the hardware object comprises coding in a high-level language.

12. The method of claim 11 wherein the high-level language comprises at least one of C, C++, SystemC, and Java.

13. The method of claim 1 wherein the hardware object comprises coding in low-level assembly code.

14. The method of claim 8 wherein the transactor comprises an abstract interface and a pin-level interface, the abstract interface being in communication with an execution environment and the pin-level interface being in communication with the hardware object.

15. The method of claim 8 wherein the hardware object, in communication with the transactor, comprises a representation of a hardware device.

16. An apparatus for executing a simulation of a hardware device, the apparatus comprising:

at least one update object having update initialization criteria;

at least one hardware object simulating functionality associated with at least one hardware device, the at least one hardware object being

responsive to the at least one update object;

at least one master object in communication with the at least one update object and the at least one hardware object, the at least one master object being configured to advance the at least one update object by a predetermined increment and thereby cause execution of the at least one hardware object based at least in part on the incremented update object.

17. The apparatus of claim 16 wherein the update object comprises a clock object.

18. The apparatus of claim 16 wherein the update object comprises a level object.

19. The apparatus of claim 16 wherein the update object comprises an arbitrary function object.

20. The apparatus of claim 17 wherein the update initialization criteria comprise at least one of a clock period, a clock duty cycle, a clock initial value, and a clock offset.

21. The apparatus of claim 18 wherein the update initialization criteria comprise at least one of a level initial value and a level transition time.

22. The apparatus of claim 19 wherein the update initialization criteria comprises a predetermined value corresponding to a predetermined time.

23. The apparatus of claim 16 further comprising the at least one transactor object associated with the hardware object.

24. The apparatus of claim 16 wherein the predetermined increment varies based at least in part on the at least one update object.

29. The apparatus of claim 23 wherein the transactor comprises an abstract

interface and a pin-level interface, the abstract interface being in communication with an execution environment and the pin-level interface being in communication with the hardware object.

30. The apparatus of claim 23 wherein the hardware object, in communication with the transactor, comprises a representation of a hardware device.